REMARKS

Applicants have received the final Office action dated November 1, 2006, in which the Examiner again rejected claims 1-27 as allegedly obvious over Dell et al. (U.S. Pat. No. 6,092,146, hereinafter "Dell") in view of Huang et al. (U.S. Pat. No. 5,008,885, hereinafter "Huang").

With this Preliminary Amendment, Applicants amend claims 1, 8, 16-17 and 21. Reconsideration is respectfully requested.

I. DELL DOES NOT TEACH MEMORY ERROR INSERTION

The final Office action, as well as the previous Office actions, takes the position that Dell teaches memory error insertion. For example, the final Office action states:

> This is because Dell performed [sic] the ***SIMMS memory error insertion, detection, and correction means used to test memory modules*** ... via its plurality of data lines into the EEPROM.

(Office action of November 1, 2006, Page 5, first full paragraph (emphasis original, internal citations omitted)). However, **Dell does not teach memory error insertion**. The cited location is reproduced below for convenience of the discussion.

> Referring, once again, to FIG. 5, once the SIMMs are inserted and the DIP switches are set, the memory adapter of the present invention is inserted into a computer system which requires unbuffered 168-pin DRAM DIMMs. When the computer system is turned on and a Power-On-Reset POR occurs, the logic 500 reads the SIMM presence detects (PDs) and the DIP switch positions in step 502. After step 502, the logic advances to step 504 where it tests to determine if two non-ECC (Error Correction Code) SIMMs are present. ECC generally involves the **generation of a special series of bits which code a data byte**. The computer system's motherboard or memory adapter must have additional circuitry for producing and comparing the ECC bits for each data transfer. Accordingly, if two non-ECC SIMMs are NOT present, the logic advances to step 506 where EEPROM 106 is turned off. However, if two non-ECC SIMMs are present, EEPROM 106 is programmed via tables 2.1, 2.2, 3.1, 3.2, 4.1, 4.2, and 4.3 by logic device 114 and the I^2 C bus controller 112 in step 508. The programming of EEPROMs is conventional and will not be described hereinafter. After step 508, the logic ends and the EEPROM, if programmed, may now be read

> by the computer system in the standard way that the Serial Presence Detects (SPDs) are read for DIMMs and the computer system may finish booting normally. In this manner, the logic device 114 serves to program the EEPROM 106 with the required SPDs so as to allow the computer system to properly access the SIMMs. The pin layouts of DIMM and SIMM sockets are conventional and connections there between known. The adapter 100 of the present invention includes hardwire connections between the pin configurations of the DIMM socket and the SIMMs.

(Dell Col. 4, line 55 through Col. 5, line 20 (emphasis added)). As close as can be determined from the final and previous Office actions, reliance is placed on the emphasized wording "generation of a special series of bits which code a data byte" as the portion of Dell alleging relating to memory error insertion; however, from the context of the citation it is clear that the generation discussed is not generation and/or insertion of errors, but generation of the codes used only to detect and correct errors.

Thus, the motivation to consider Dell with Huang discussed in the Office action is without basis, as the primary factor relied upon is the nonexistent memory error insertion of Dell. Huang does not remedy the deficiency of Dell. For this reason alone the rejections should be withdrawn.

II. CLAIM REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly obvious over Dell and Huang. Applicants amend claim 1 place the term "memory module" in the body of the claim to ensure that memory module is considered a limitation of the claim, and to more clearly define over the internal error insertion of Huang.

Claim 1 specifically recites, "a memory module comprising: a plurality of memory circuits, wherein at least one of the memory circuits comprises a serial presence detect (SPD) memory circuit; a plurality of data lines that transfer the data to and from the plurality of memory circuits; and testing logic coupled to at least one of the plurality of data lines, wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error into one or more of the plurality of data lines, the injecting externally of the memory circuits." Applicants

respectfully submit that Dell and Huang do not teach or suggest such a system. First and foremost, there is no motivation to combine Dell and Huang, as contrary to the assertion of the Office action, Dell does not contemplate memory error insertion.

Moreover, in Huang errors are inserted into logic of a monolithic integrated circuit (Huang Col. 48-51; Figure 1), not data lines of a memory module. Thus, even if hypothetically Dell is properly considered with Huang (which Applicants do not admit), Dell and Huang fail to teach a "testing logic coupled to at least one of the plurality of data lines, wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error into one or more of the plurality of data lines, the injecting externally of the memory circuits." Contrary to the assertion of the final Office action, Applicants are not suggesting that Dell fails to teach data lines; rather, Applicants submit that even if Dell and Huang are considered together, the two references fail to teach the claim limitations because the error insertion in Huang is within the monolithic integrated circuit.

Based on the foregoing, Applicants respectfully submit that claim 1 is not rendered unpatentable by Dell and Huang, and that claim 1 should be allowed together with all claims which depend from claim 1 (claims 2-7).

B. Claim 8

Claim 8 stands rejected as allegedly obvious over Dell and Huang. Applicants amend claim 8 to more clearly define over the "support processor" of Huang, which is clearly external to the circuit under test.

Claim 8 specifically recites, "sending a request to inject a memory error into a data line external of a memory module, the sending by an application program executed by a computer system; receiving the request to inject the error into the data line of a memory module, the receiving by a testing logic integrated with the memory module in the computer system; and injecting the error into the data line by a testing logic integrated with the memory module." Applicants respectfully submit that Dell and Huang do not teach or suggest such a system. Huang teaches inserting errors within integrated monolithic integrated circuits;

however, it appears that the injecting is controlled by an external "support processor."

> The support processor may be an entity which is external to the processing machine 8, yet which has access to the machine through the software which controls it.

(Huang Col. 4, lines 44-47; Figure 1). Thus, even if the teachings of Dell are precisely as office action suggests (which Applicants do not admit), Dell and Huang still fail to teach the limitations of claim regarding "sending a request to inject a memory error into a data line external of a memory module, the sending by an application program executed by a computer system; receiving the request to inject the error into the data line of a memory module, the receiving by a testing logic integrated with the memory module in the computer system."

Based on the foregoing, Applicants respectfully submit that claim 8 is not rendered unpatentable by Dell and Huang, and that claim 8 should be allowed together with all claims which depend from claim 8 (claims 9-15).

C. Claim 16

Claim 16 stands rejected as allegedly obvious over Dell and Huang. Applicants amend claim 8 to more clearly define over the "support processor" of Huang, which is clearly external to the circuit under test.

Claim 16, by contrast, specifically recites, "A computer readable media storing instructions executable by a processor in a computer system to implement a method comprising: receiving data from a serial presence detect (SPD) device associated with a memory device, the memory device within the computer system; generating an error injection procedure by the processor based in part on the received data; and applying a bias voltage on at least one data line coupled to the memory device based on the error injection procedure." Applicants respectfully submit that Dell and Huang do not teach or suggest such a system. Huang teaches inserting errors from within integrated monolithic integrated circuits; however, it appears that the injecting is controlled by an external "support processor." (Huang Col. 4, lines 44-47; Figure 1). Thus, even if the teachings of Dell are precisely as office action suggests (which Applicants do not admit), Dell

and Huang still fail to teach the limitations of claim regarding controlling software executed within the same computer system as the memory device

Based on the foregoing, Applicants respectfully submit that claim 16 is not rendered unpatentable by Dell and Huang, and that claim 16 should be allowed together with all claims which depend from claim 16 (claims 17-20).

D. Claim 21

Claim 21 stands rejected as allegedly obvious over Dell and Huang. Applicants amend claim 21 place the term "memory module" in the body of the claim, and to more clearly define over the internal error insertion of Huang.

Claim 21 specifically recites, "a memory module comprising: a plurality of means for storing data, wherein at least one of the means for storing comprises a serial presence detect (SPD) memory circuit; a plurality of means for transferring data to and from the plurality of means for storing data; and a means for applying a bias voltage coupled to the plurality of means for storing data, wherein the means for applying a bias voltage utilizes data stored in the SPD memory circuit to inject an error into at least one of the plurality of means for transferring data, the applying voltage external to the plurality of means for storing." Applicants respectfully submit that Dell and Huang do not teach or suggest such a system. First and foremost, there is no motivation to combine Dell and Huang, as contrary to the assertion of the Office action, Dell does not contemplate memory error insertion, for reasons discussed above in Section I.

Moreover, in Huang errors are inserted into logic of a monolithic integrated circuit (Huang Col. 48-51; Figure 1), not into means for transferring data of a memory module. Thus, even if hypothetically Dell is properly considered with Huang (which Applicants do not admit), Dell and Huang fail to teach "a means for applying a bias voltage coupled to the plurality of means for storing data, wherein the means for applying a bias voltage utilizes data stored in the SPD memory circuit to inject an error into at least one of the plurality of means for transferring data." Contrary to the assertion of the final Office action, Applicants are not suggesting that Dell fails to teach data lines; rather, Applicants submit that even if Dell and Huang are considered together, the two references fail to teach applying

bias voltage to a means for transferring data, as the error insertion in Huang is effected within the monolithic integrated circuit.

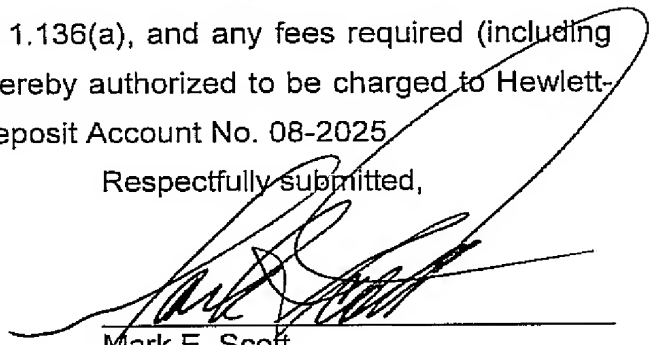
Based on the foregoing, Applicants respectfully submit that claim 21 is not rendered unpatentable by Dell and Huang, and that claim 21 should be allowed together with all claims which depend from claim 21 (claims 22-27).

III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



Mark E. Scott
PTO Reg. No. 43,100
CONLEY ROSE, P.C.
(512) 391-1900 (Phone)
(512) 320-9181 (Fax)
ATTORNEY FOR APPLICANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400